數位系統 Digital Systems 資訊工程系四進二A 課號 3578

Instructor: 洪士程 副教授

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Room:理工大樓E726

Tel: 7801

Course Time & Office Hours

- **Course Time**
- Friday A,B,C (18:25 20:45)
- Classroom: G-106
- Office Hours
- Wednesday 10:25-12:10

Credits

- Required or Elective
 - Required (必修)
- Credits
 - 3 Credits (三學分)

Goal

- An basic knowledge of digital systems.
- Give an introduction to:
- basic aspects and electronic aspects of logic circuits
- optimized implementation of logic functions
- combinational circuits used as building blocks
- storage elements
- synchronous and asynchronous sequential circuits

Text Book

M. M. Mano and M. D. Ciletti, "Digital Design," 5th edition., Pearson Prentice Hall, 2013.

Reference Books

Reference:

Jr. Charles H. Roth, Larry L. Kinny,

"Fundamentals of Logic Desugn", 7th edtion, CL Engineering, 2013.

Schedule of Progress (1/3)

- Introduction to course (week 1)
- Chap 1 Introduction (week 1)
- Chap 1 Binary Numbers (week 2)
- Chap 1 Complements of Numbers (week 3)
- Chap 2 Basic Theorems and Properties of Boolean Algebra (week 4)
- Chap 2 Canonical and Standard Forms (week 5)
- Chap 2 Logic Gates (week 6)

Schedule of Progress (2/3)

- Chap 3 Gate-Level Minimization The Map Method (week 7)
- Chap 3 Product-of-Sums Simplification (week 8)
- Midterm exam (week 9)
- Chap 3 NAND and NOR Implementation (week 10)
- Chap 3 Hardware Description Language (week 11)
- Chap 4 Combinational Circuits (week 12)

Schedule of Progress (3/3)

- Chap 4 Combinational Logic Analysis Procedure (week 13)
- Chap 4 Combinational Logic Design Procedure (week 14)
- Chap 5 Synchronous Sequential Logic Sequential Circuits (week 15)
- Chap 5 Synchronous Sequential Logic Analysis of Clocked (week 16)
- Chap 5 State Reduction and Assignment (week 17)
- Final exam (week 18)

Resources

- Text Book
- Handout

http://lms.ctl.cyut.edu.tw/

LMS-數位學習系統

Evaluation

- Quiz (30%)
- Participation (10%)
- Mid exam (30%)
- Final exam (30%)