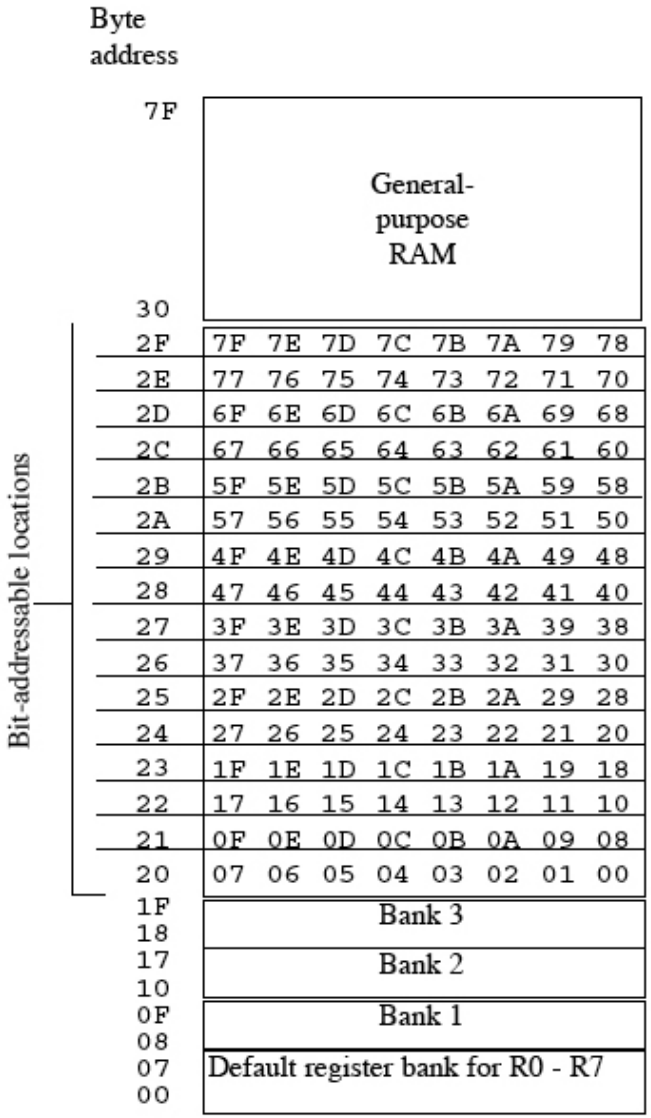
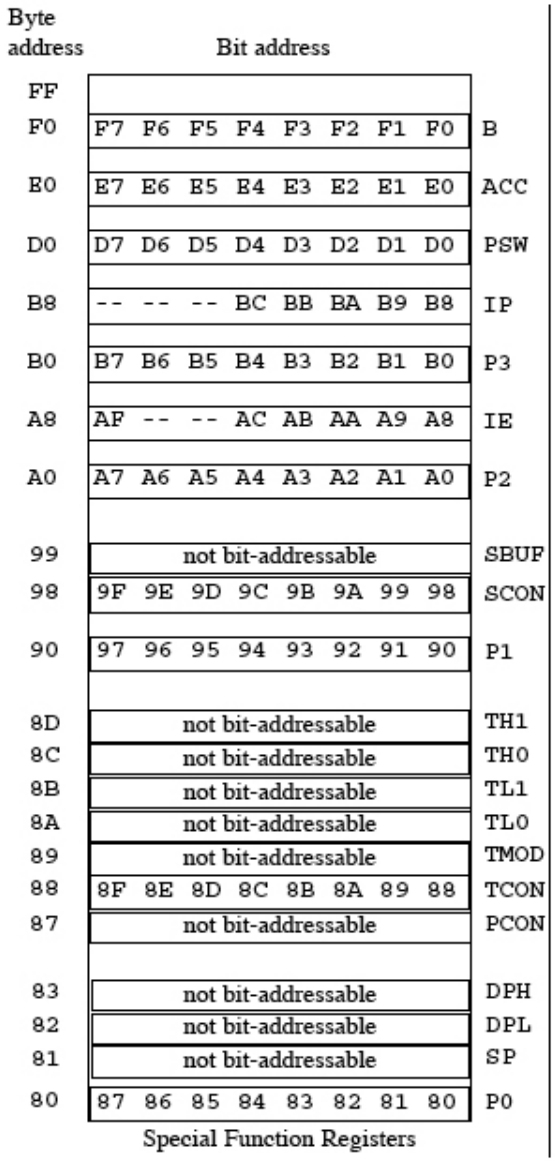
Figure 5–1 16 Bytes of Internal RAM. Note: They are both bit- and byte-accessible.



© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Figure 5–2 SFR RAM Address (Byte and Bit)



© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

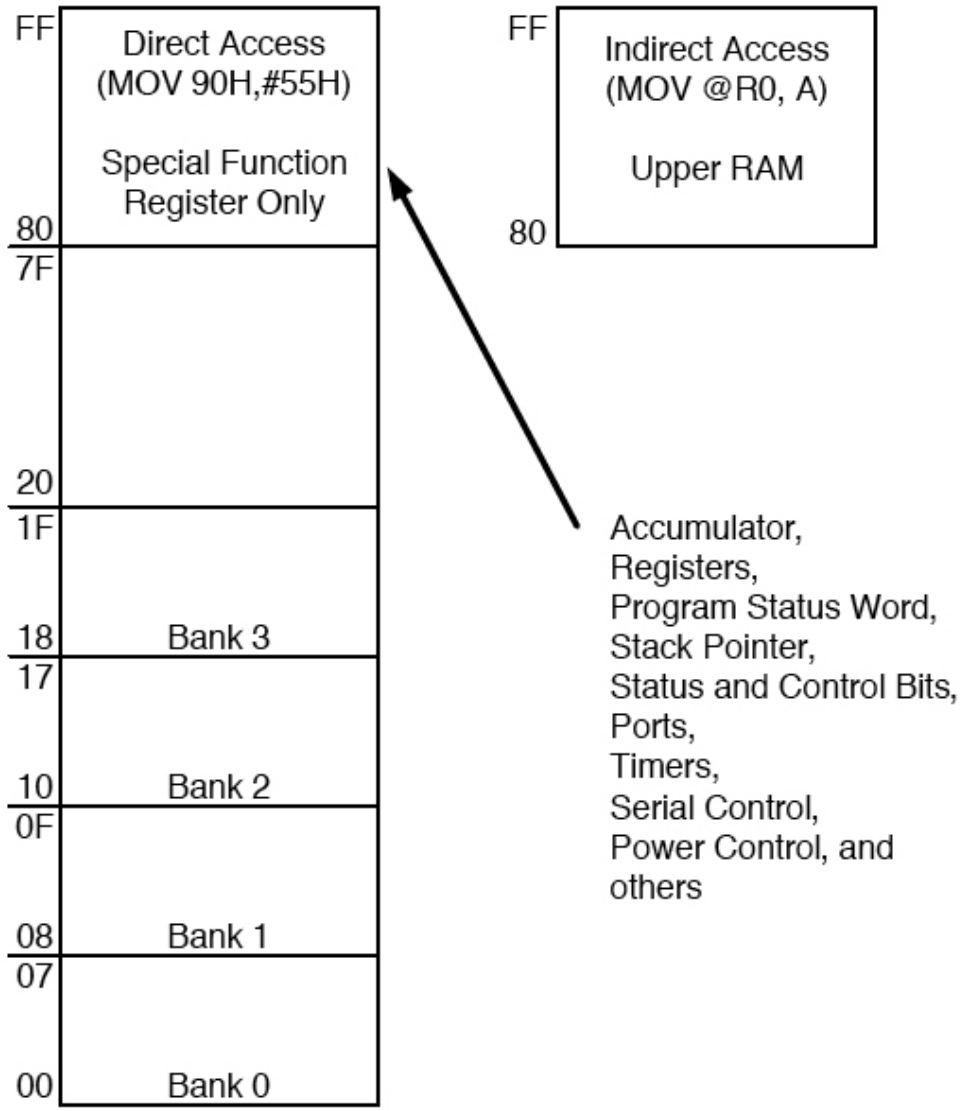
Figure 5–3 Bits of the PSW Register

CY	AC	F0	RS1	RS0	OV	--	P

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

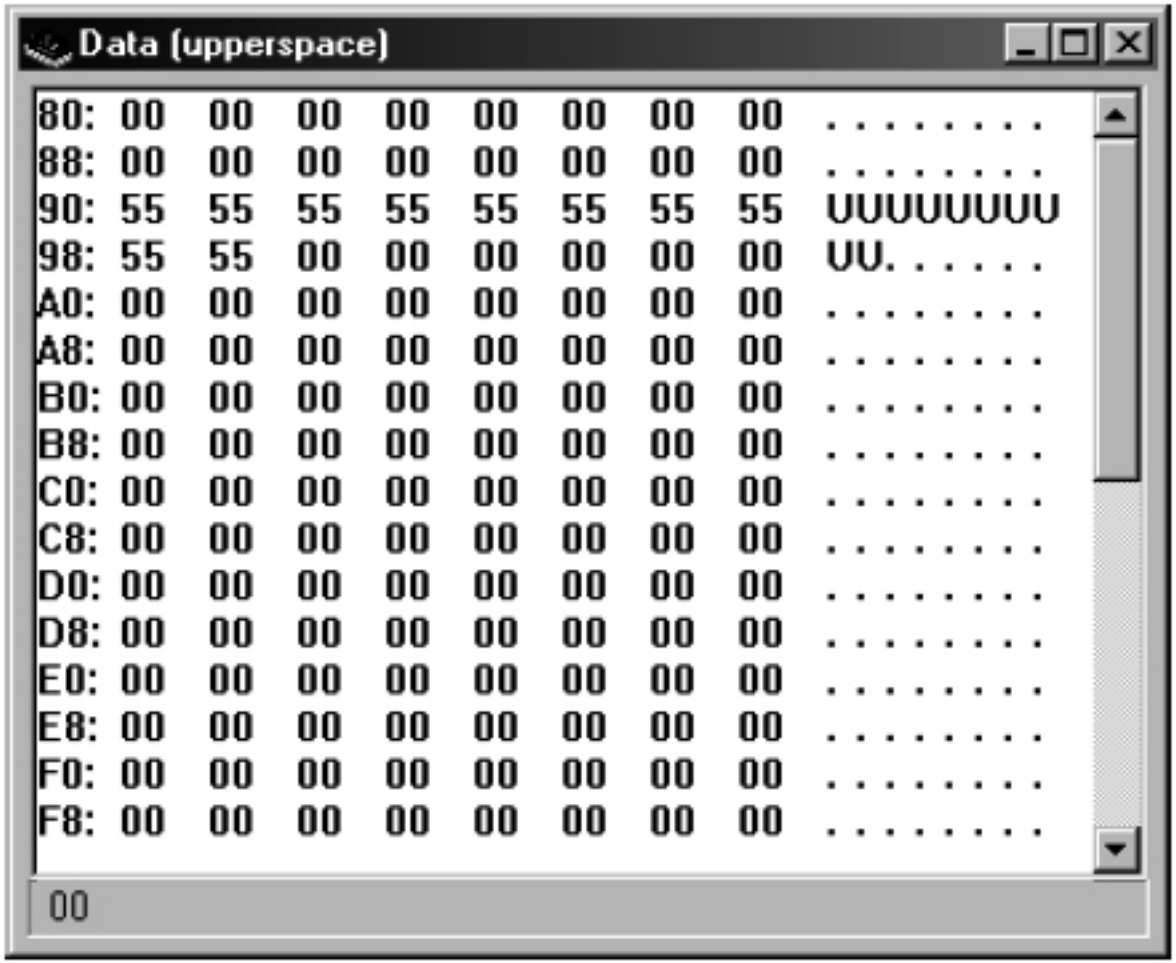
© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Figure 5–4 8052 On-Chip RAM Address Space



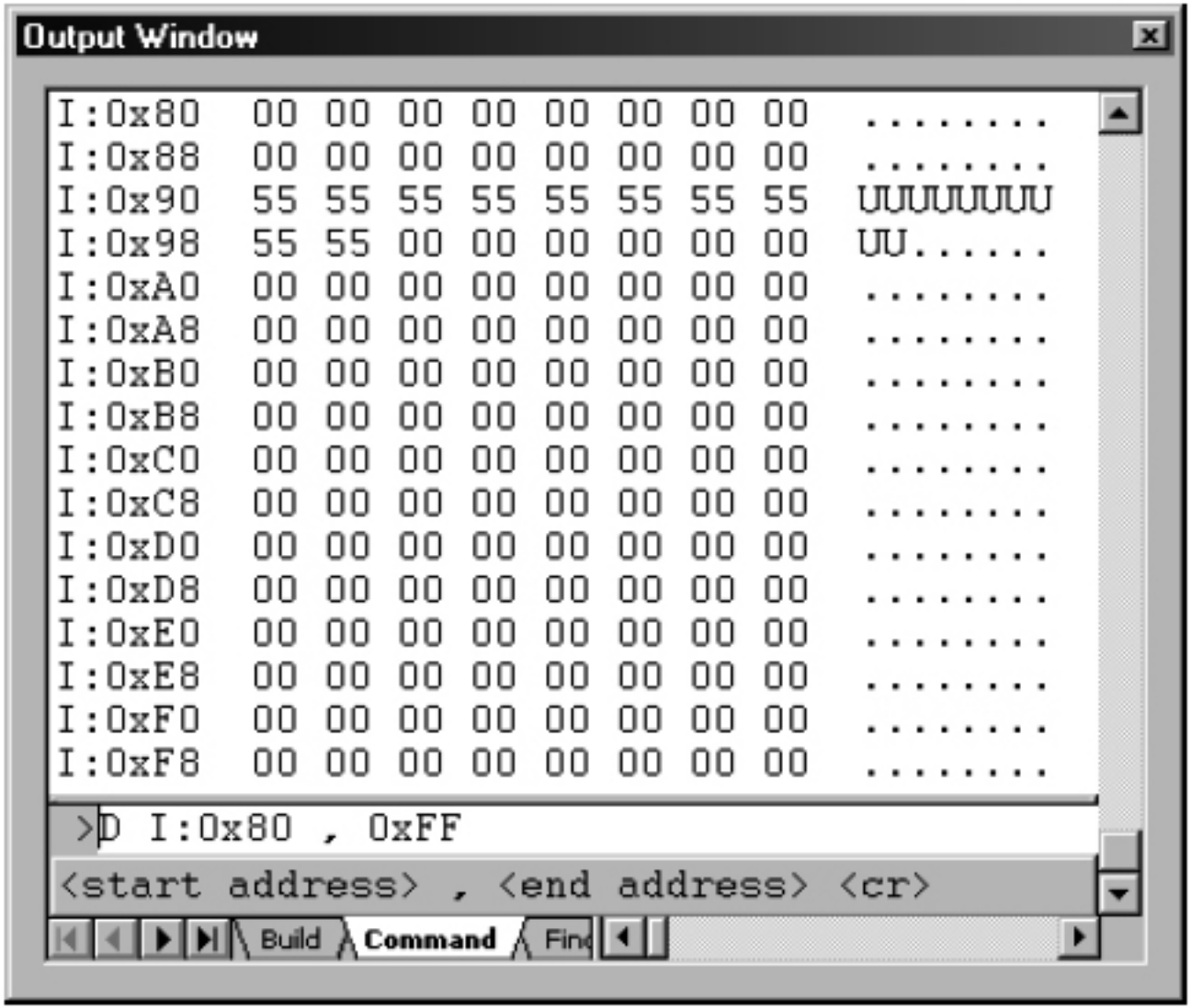
© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Figure 5–5. Franklin Software's ProView Upper Memory for the 8052



© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Figure 5–6. Keil's μ Vision Upper Memory for the 8052



© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Table 5–1 8051 Special Function Register (SFR) Addresses

Symbol	Name	Address
ACC*	Accumulator	0E0H
B*	B register	0F0H
PSW*	Program status word	0D0H
SP	Stack pointer	81H
DPTR	Data pointer 2 bytes	
DPL	Low byte	82H
DPH	High byte	83H
P0*	Port 0	80H
P1*	Port 1	90H
P2*	Port 2	0A0H
P3*	Port 3	0B0H
IP*	Interrupt priority control	0B8H
IE*	Interrupt enable control	0A8H
TMOD	Timer/counter mode control	89H
TCON*	Timer/counter control	88H
T2CON*	Timer/counter 2 control	0C8H
T2MOD	Timer/counter mode control	0C9H
TH0	Timer/counter 0 high byte	8CH
TL0	Timer/counter 0 low byte	8AH
TH1	Timer/counter 1 high byte	8DH
TL1	Timer/counter 1 low byte	8BH
TH2	Timer/counter 2 high byte	0CDH
TL2	Timer/counter 2 low byte	0CCH
RCAP2H	T/C 2 capture register high byte	0CBH
RCAP2L	T/C 2 capture register low byte	0CAH
SCON*	Serial control	98H
SBUF	Serial data buffer	99H
PCON	Power control	87H

* Bit-addressable

© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Table 5–2 Single-Bit Instructions

Instruction		Function
SETB	bit	Set the bit (bit = 1)
CLR	bit	Clear the bit (bit = 0)
CPL	bit	Complement the bit (bit = NOT bit)
JB	bit,target	Jump to target if bit = 1 (jump if bit)
JNB	bit,target	Jump to target if bit = 0 (jump if no bit)
JBC	bit,target	Jump to target if bit = 1, clear bit (jump if bit, then clear)

© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458

Table 5–3 Bit Addresses for All Ports

P0	Addr	P1	Addr	P2	Addr	P3	Addr	Port's Bit
P0.0	80	P1.0	90	P2.0	A0	P3.0	B0	D0
P0.1	81	P1.1	91	P2.1	A1	P3.1	B1	D1
P0.2	82	P1.2	92	P2.2	A2	P3.2	B2	D2
P0.3	83	P1.3	93	P2.3	A3	P3.3	B3	D3
P0.4	84	P1.4	94	P2.4	A4	P3.4	B4	D4
P0.5	85	P1.5	95	P2.5	A5	P3.5	B5	D5
P0.6	86	P1.6	96	P2.6	A6	P3.6	B6	D6
P0.7	87	P1.7	97	P2.7	A7	P3.7	B7	D7

© 2006 Pearson Education, Inc.
Pearson Prentice Hall
Upper Saddle River, NJ 07458