Figure 4–1 8051 Pin Diagram

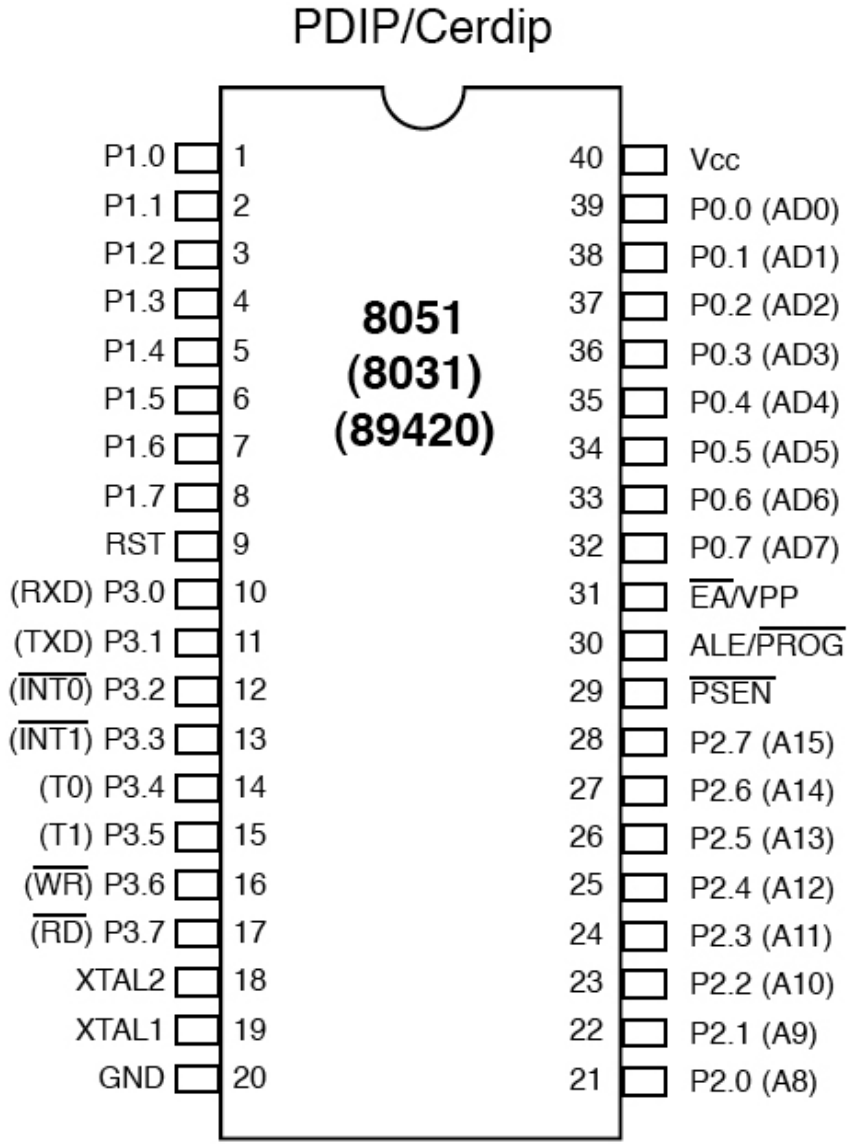

Figure 4–2 Port 0 with Pull-Up Resistors

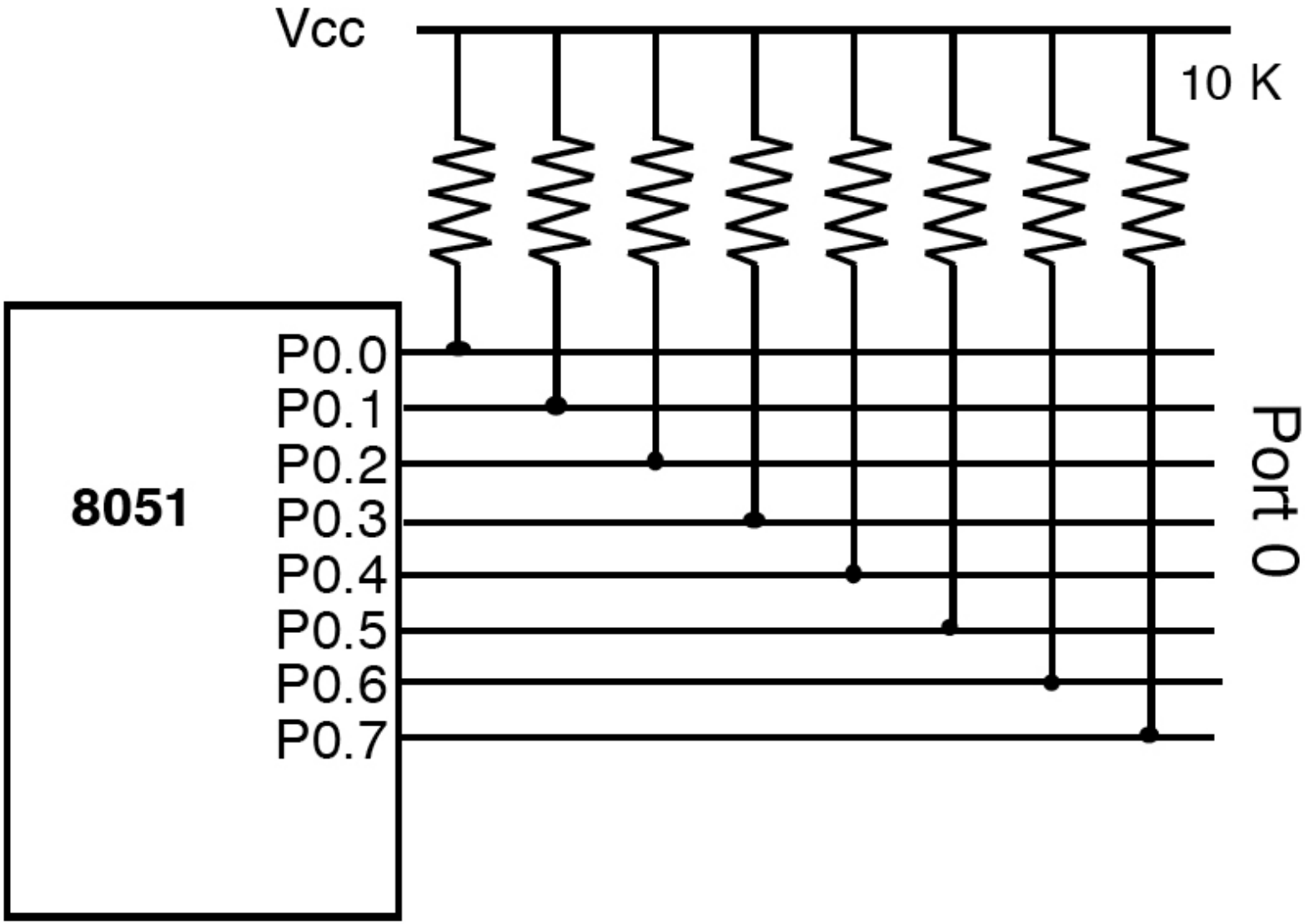

Table 4–1 Port 3 Alternate Functions

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17

Table 4–2 Reset Value of Some 8051 Ports

Register	Reset Value (Binary)
P0	11111111
P1	11111111
P2	11111111
P3	11111111

Table 4–3 Single-Bit Addressability of Ports

P0	P1	P2	P3	Port Bit
P0.0	P1.0	P2.0	P3.0	D0
P0.1	P1.1	P2.1	P3.1	D1
P0.2	P1.2	P2.2	P3.2	D2
P0.3	P1.3	P2.3	P3.3	D3
P0.4	P1.4	P2.4	P3.4	D4
P0.5	P1.5	P2.5	P3.5	D5
P0.6	P1.6	P2.6	P3.6	D6
P0.7	P1.7	P2.7	P3.7	D7

Table 4–4 Single-Bit Instructions

Instruction		Function
SETB	bit	Set the bit (bit = 1)
CLR	bit	Clear the bit (bit = 0)
CPL	bit	Complement the bit (bit = NOT bit)
JB	bit,target	Jump to target if bit = 1 (jump if bit)
JNB	bit,target	Jump to target if bit = 0 (jump if no bit)
JBC	bit,target	Jump to target if bit = 1, clear bit (jump if bit, then clear)

Table 4–5 Instructions For Reading an Input Port

Mnemonic	Example	Description
`MOV A, PX`	`MOV A, P2`	Bring into A the data at P2 pins
`JNB PX.Y,..`	`JNB P2.1, TARGET`	Jump if pin P2.1 is low
`JB PX.Y,..`	`JB P1.3, TARGET`	Jump if pin P1.2 is high
`MOV C, PX.Y`	`MOV C, P2.4`	Copy status of pin P2.4 to CY

Table 4–6 Instructions Reading a Latch (Read-Modify-Write)

Mnemonic		Example	
ANL	Px	ANL	P1,A
ORL	Px	ORL	P2,A
XRL	Px	XRL	P0,A
JBC	PX.Y,TARGET	JBC	P1.1,TARGET
CPL	PX.Y	CPL	P1.2
INC	Px	INC	P1
DEC	Px	DEC	P2
DJNZ	PX.Y,TARGET	DJNZ	P1,TARGET
MOV	PX.Y,C	MOV	P1.2,C
CLR	PX.Y	CLR	P2.3
SETB	PX.Y	SETB	P2.3

Note: x is 0, 1, 2, or 3 for P0 - P3.